## AMENDMENTS TO THE CLAIMS

*Listing of Claims*

A listing of the entire set of pending claims is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method of manufacturing a source-gated transistor, including:
(a) providing a transparent substrate [[(2)]];
(b) depositing a gate layer and patterning the gate layer to form a gate [[(4)]];
(c) depositing a gate insulating layer [[(6)]];
(d) depositing a thin film semiconductor layer [[(8)]];
(e) depositing a transparent source layer ~~(18)~~ defining a barrier with the semiconductor layer [[(8)]], using a step of back exposure through the substrate using the gate [[(4)]] as a mask to define the barrier between source layer ~~(18)~~ and the semiconductor layer [[(8)]];
(f) depositing a positive photoresist layer;
(g) exposing the positive photoresist layer through the transparent substrate and source layer using the gate as a mask to pattern the photoresist in self-alignment with the gate;
(h) etching the transparent source layer to form a source region using the pattern defined directly or indirectly by the photoresist layer;
(i) forming spacers at the edge of the source region; and
(j) implanting dopants into drain regions of the semiconductor layer using the source region and spacers as a mask to form highly doped drain regions spaced from the source region by the width of the spacers.

2. (Currently Amended) A method according to claim 1, further comprising:
defining a drain region ~~(24)~~ in the semiconductor layer in contact with a drain contact;
wherein spacers ~~(28)~~ are used to define the lateral extent of a spacer region ~~(32)~~ of the semiconductor layer ~~(8)~~ in registration with the gate ~~(4)~~ using a self-aligned process, the spacer region ~~(32)~~ being the region between the drain region ~~(24)~~ and the barrier.

3. (Cancelled)

4. (Currently Amended) A method according to ~~any preceding~~ claim 1, further comprising the step of defining at least one field relief region ~~or regions (32, 48)~~ at the edge of the source region in registration with the gate ~~(4)~~ using a self-aligned back exposure process, wherein ~~in which~~ the field relief region is ~~or regions are~~ patterned using photoresist on the top of the substrate exposed with illumination passing through the substrate ~~(2)~~ using the gate ~~(4)~~ as a mask.

5. (Cancelled)

6. (Currently Amended) A method according to claim ~~5~~ 1, further comprising, after step (d): ~~including~~

depositing an insulating layer ~~(10) after step (d) of the depositng the semiconductor layer (8);~~ and

etching the insulating layer ~~(10)~~ to form a source window ~~(14)~~ in alignment with the mask.

7. (Currently Amended) A method according to claim ~~5 or 6~~ 1, further comprising:

depositing a transparent sacrifical layer ~~(20)~~ on the transparent source layer ~~(18)~~ before carrying out steps ~~(f) and (g)~~ of depositing and patterning the positive photoresist layer ~~(22)~~;

after carrying out step (g), forming spacers ~~(28)~~ on the sidewalls of the transparent sacrificial layer ~~(20)~~ so that the spacers ~~(28)~~ and transparent sacrificial layer ~~(20)~~ are together wider than the gate; and

using the transparent sacrificial layer ~~(20)~~ and spacers ~~(28)~~ as a mask to etch the source layer ~~(18)~~ and the underlying insulating layer ~~(10)~~ to leave the source layer extending over a region wider than the gate and to form the insulating layer to define a field plate spacer ~~(10~~) between the source layer ~~(18)~~ and the semiconductor layer [[(8)]].

8. (Currently Amended) A method according to claim ~~5~~ 1 wherein step (i) of forming spacers is carried out after the step (h) of forming the source region so that the spacers are formed on the edges of the source region.

9. (Currently Amended) A method according to ~~any of claims 5 to 8~~ claim 1, further comprising performing an implant into the semiconductor layer ~~(8)~~ after step (h) of forming the source region to form a doped region ~~(32)~~ of the semiconductor layer [[(8)]] in alignment with the source region ~~(18)~~.

10. (Currently Amended) A method according to ~~any preceding~~ claim 1, further comprising depositing a barrier-lowering implant ~~(16)~~ in the semiconductor layer [[(8)]].

11. (Currently Amended) A method according to claim 10 wherein the barrier lowering implant is self-aligned to the gate but implanted over a narrower area than the area of the gate defining a field relief region ~~(48)~~ of the central region around the barrier lowering implant which is not implanted with the barrier lowering implant.

12. (Currently Amended) A method according to ~~any preceding~~ claim 1, further comprising depositing a transparent insulating layer ~~(42)~~ in the central region at the centre of the barrier between the source region ~~(18)~~ and semiconductor layer [[(8)]].

13-16. (Cancelled)